AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1-8 (Canceled)

Claim 9 (Currently Amended): A method of designing a semiconductor device, comprising:

a step of measuring a thickness of a pad oxide film formed on a surface of a semiconductor substrate and a thickness of a nitride film formed on said pad oxide film;

a step of measuring an internal stress of said nitride film;

a step of measuring ~~the~~ a width of a device formation region formed on said semiconductor substrate and a width of a device isolation region adjacent to said device formation region;

a step of measuring a depth of a groove formed inside said semiconductor substrate by etching a portion existing on said device isolation region among ~~a nitride~~ said nitride film formed on said oxide film;

a step of conducting stress analysis using said thickness of a pad oxide film, said thickness of a nitride film, said width of a device formation region, said width of a device isolation region, said depth and said internal stress and obtaining an internal stress estimated to occur due to thermal oxidation in the proximity of said groove;

a step of preparing a design chart representing a region in which a quotient obtained by dividing said internal stress and said internal estimated stress by a

dislocation occurrence limit stress, at which dislocation occurs due to thermal oxidation, exceeds 1, by using the width of said device formation region and the width of said device isolation region as parameters; and

a step of setting a value of the width of said device formation region and a value of the width of said device isolation region, at which dislocation does not occur, in design of said semiconductor substrate.

Claim 10 (Original): A method of designing a semiconductor device according to claim 9, wherein said groove has a thermal oxidation film formed by thermal oxidation, and which further includes:

a step of applying data of said design chart so as to establish the following formula relating to a dislocation occurrence limit stress value due to thermal oxidation in said device formation region and said device isolation region adjacent to one another:

$$\sigma/\sigma_c = [\{0.78 + 0.054D - 0.00086D^2\} + \{-0.040t_p + 0.00086t_p^2\} + \{0.01t_n + 0.000051t_n^2\}] \times [0.043 + 0.61L - 0.14L^2 + 0.015L^3] \times [1.4 - 0.49S + 0.18S^2 - 0.021S^3] \leq 1$$

wherein L/S in a value of said ratio, t_p is the thickness of said pad oxide film, t_n is the thickness of said nitride film and D is the depth of said groove.

Claim 11 (Original): A method of designing a semiconductor device according to claim 9, which further includes:

a step of deciding an etch-back distance of said pad oxide film not causing the occurrence of dislocation by using said design chart; and

a step of etching and removing said pad oxide film by said etch-back distance in a direction parallel to the surface of said semiconductor substrate.

Claim 12 (Currently Amended): A method of designing a semiconductor device comprising:

a step of measuring a thickness of a pad oxide film formed on a surface of a semiconductor substrate, and a thickness of a nitride film formed on said pad oxide film;

a step of measuring an internal stress of said nitride film;

a step of measuring a width of a device formation region formed on said semiconductor substrate, and a width of a device isolation region adjacent to said device formation region;

a step of measuring a depth of a groove formed in said semiconductor device by etching a portion of said nitride film formed on said pad oxide film and existing on said device isolation region;

a step of conducting stress analysis by using said thickness of a pad oxide film, said thickness of a nitride film, said width of a device formation region, said width of a device isolation region, said depth and said internal stress, and obtaining an internal stress estimated to occur due to thermal oxidation in the proximity of said groove;

a step of preparing a stress distribution chart representing a region, in which said internal stress and said internal estimated stress exceeds a dislocation occurrence limit stress at which dislocation occurs due to thermal oxidation, by using the width of said device formation region and the width of said device isolation region as parameters; and

a step of setting the width of said device formation region and the width of

said device isolation region not causing dislocation by using said stress distribution chart in designing said semiconductor substrate.

Claims 13-29. (Canceled)